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Sarnoff Europe joins the TSMC Design Center Alliance with its ESD Design portfolio

GISTEL, Belgium (September 23, 2008) – Sarnoff Europe (www.sarnoffeurope.com) today announced that it has joined the TSMC Design Center Alliance (DCA). The DCA program helps align IC companies and TSMC-qualified providers.

Under the DCA program, Sarnoff Europe will further expand its on-chip ESD protection for applications in standard and high voltage CMOS. Since 2007, twenty four high-volume product ICs have been released to TSMC's 65nm process technologies using Sarnoff's ESD protection IP and the 40nm G silicon verified ESD solutions were released last month.

By adding the Sarnoff ESD to its DCA program, TSMC continues to strengthen its commitment to help customers achieve time-to-market and return on investment as part of TSMC's Open Innovation Platform™. The TSMC Open Innovation Platform efficiently and openly encourages the speedy implementation of innovation amongst the semiconductor design community. A key element is a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that more efficiently empowers innovation throughout the supply chain.

"Sarnoff Europe combines IP in an advanced design flow with calculation and integration tools, and customized services. They complement the diverse Design Services offered by our portfolio of DCA partners," said Tom Quan, Deputy Director at the Design Methodology and Service Marketing at TSMC.

The Sarnoff Europe ESD portfolio focuses primarily on advanced low-leakage and low-capacitive solutions for high-speed, wireless, SerDes, USB, Gigabit Ethernet, PCI Express, Serial ATA applications. In addition, the company provides high (8kV) ESD robustness for such challenging applications as HDMI and DisplayPort products.

The "TakeCharge Design Kit" offers complete solution sets for I/O and full-chip ESD protection including scalable GDSII cells. It focuses heavily on the ESD design flow with a full tool suite for calculation and integration in the overall IC design. Detailed layout documentation and extensive training teaches engineers to independently integrate advanced ESD solutions in their custom IC design, and successfully tape-out a new IC.

The "TakeCharge Design Solutions" package focuses on providing "single-chip" ESD designs with a very fast turnaround time of approximately three weeks.

Sarnoff Europe's ESD solutions are fully qualified for industry standard specifications, meeting 2,000V Human Body Model (HBM) and 200V Machine Model (MM) even for the highest speed pins, RF, analog, mixed signal and other low cap applications – and are product proven down to

65nm CMOS with silicon proven solutions for the TSMC 40nm G process node. Charged Device Model (CDM) requirements are also covered.

"Sarnoff Europe is excited and honored to cooperate with TSMC," said Koen Verhaege, Executive Director of Sarnoff Europe. "Our mission is to empower customers with advanced solutions and tools so they can independently perform successful ESD design, getting it right the first time, every time, regardless of the complexity of the process, application or innovation. More than 450 volume production ICs to date testify to the quality and versatility of the advanced ESD solutions."

A full overview of the Sarnoff Europe ESD Solution information can be found online at http://www.tsmc.com/english/services/s010445.htm

About Sarnoff Europe
Sarnoff Europe (www.sarnoffeurope.com) headquartered in Gistel, Belgium, is a subsidiary company of Sarnoff Corporation – founded in 1942 as the RCA Laboratories. Sarnoff Europe assumes worldwide responsibility for the development and commercialization of Sarnoff's TakeCharge® on-chip ESD protection IP.

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