Thesis High Speed OVT design for memory busses

2025-02-05

Version 7

Sofics BV
RPR 0472.687.037
Brugse Baan 188A
8470 Gistel

Contact:

Joren Vaes

-

TABLE OF CONTENTS

1. General information

Thesis subject	**Thesis High Speed OVT design for memory busses**
Major	Electrical engineering, Nanodevices & circuits
Contact person	Dr. Joren Vaes jvaes@sofics.com
How to apply?	The student may contact Dr. Joren Vaes (see above)

2. Background

Memory interfaces are a crucial type of I/O in integrated circuits, with DDR (Double Data Rate) memory being one of the most widely used standards, as defined by JEDEC. The latest iteration, DDR5, operates at a supply voltage of 1.1V, compared to DDR4 at 1.2V and DDR3 at 1.5V.

Traditionally, CMOS fabrication processes have included two types of transistors: **core** devices, which typically operate at a maximum voltage of 0.85V or lower, and **I/O** transistors, designed for higher voltages (often 1.8V or 2.5V, depending on the process). These I/O transistors achieve higher voltage tolerance through the use of a thicker gate oxide.

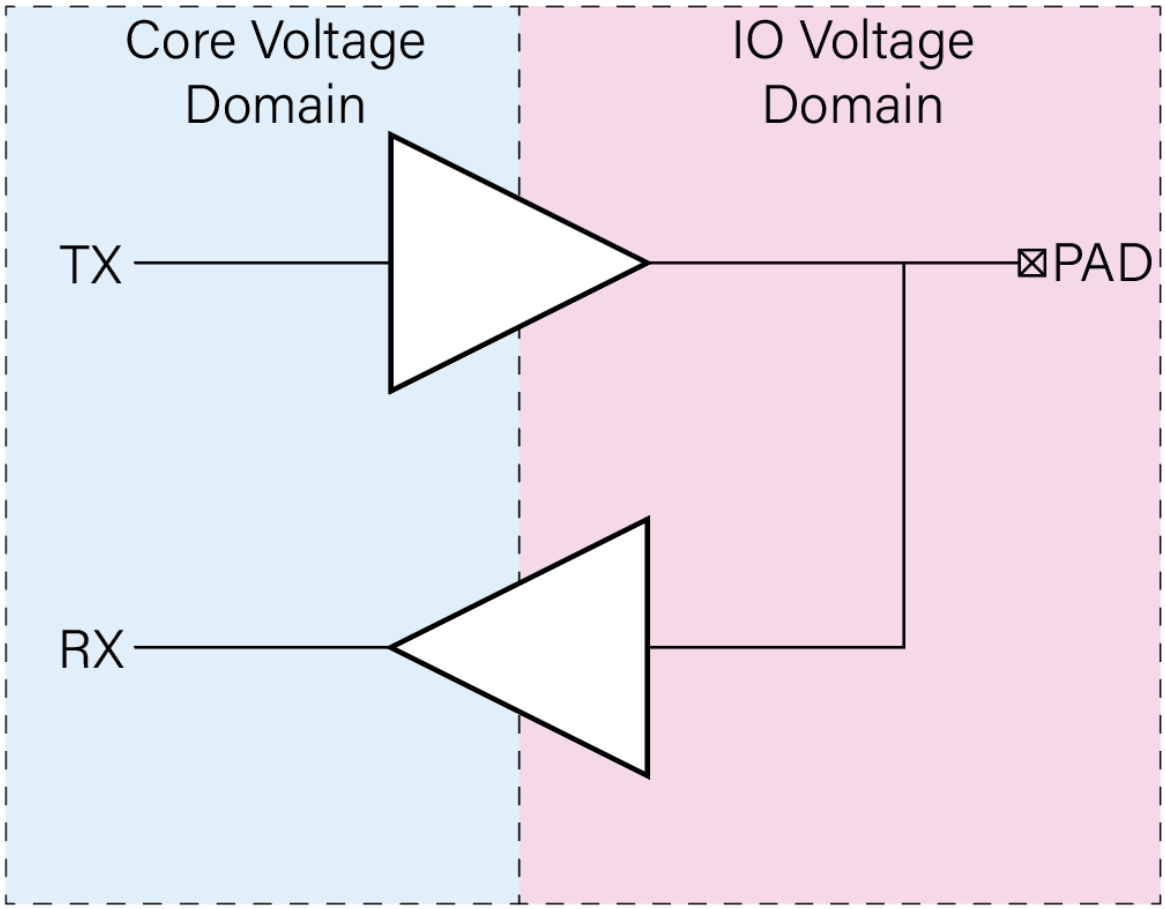
However, in gate-all-around (GAA) transistor technologies, manufacturing constraints prevent the use of multiple oxide thicknesses. As a result, only core devices are available, necessitating alternative techniques to achieve higher operating voltages. One common approach is **transistor stacking**, which ensures individual transistors remain within their safe voltage limits. While stacking is well understood for lower-speed I/Os operating at tens or hundreds of megahertz, it becomes significantly more challenging at the multi-gigabit speeds required for DDR interfaces.

3. Objective

This thesis aims to explore techniques for enabling **low-power, high-speed I/Os** that can operate at voltages exceeding the limit of a single transistor. The target is to develop an I/O capable of functioning at **up to 1.5V** (for DDR3 compatibility) while achieving speeds of **6.4 Gbaud or higher** to support DDR5.

The project will begin with a **literature review** on overvoltage-tolerant (OVT) I/Os to assess existing design techniques. Additionally, the student will conduct a study of DDR interface specifications to understand the key design requirements.

Following this, the focus will shift to the **schematic design in a 22nm CMOS or 16nm FinFET technology** of an OVT I/O meeting the defined specifications.



Expected workload:

- 15% Literature review
- 10% Specification definition
- 50% design and simulation
- 25% writing of thesis